WHAT IS CLAIMED IS:

1. A microprocessor provided with a program modification function comprising:

an instruction storage unit including a ROM for storing instructions composing a program to be processed and a modified instruction storage unit for storing a modified instruction for program modification; and

an address translation unit for receiving an instruction address of an instruction stored in said ROM and for translating the instruction address into a substitutive address at which the modified instruction is stored in said modified instruction storage unit when the instruction address matches with a modifying address which is an address of an instruction to be modified,

said address translation unit outputting the substitutive address to said instruction storage unit instead of the instruction address.

2. The microprocessor of claim 1, wherein,

said address translation unit comprises:

a modifying address storage unit for holding a value of a predetermined bit of the modifying address;

an address comparator for comparing a value of said predetermined bit of the received instruction address with the value held in said modifying address storage unit to determine

whether or not these values match with each other;

a substitutive address storage unit for holding a value of said predetermined bit of the substitutive address; and

an address selector for receiving determination results of said address comparator, outputting as a value of said predetermined bit of a new instruction address, the value held in said substitutive address storage unit when the received results indicate that these values match with each other, and otherwise, the value of said predetermined bit of the instruction address.

3. The microprocessor of claim 1, wherein said address translation unit is so composed that a bit width to be a translation target is changeable when the instruction address is translated into the substitutive address.

4. The microprocessor of claim 3, wherein said address translation unit comprises:

a modifying address storage unit for holding a value of a predetermined bit of the modifying address;

an address comparator for comparing a value of said predetermined bit of the instruction address with the value held in said modifying address storage unit to determine whether or not these values match with each other;

a substitutive address storage unit for holding a value

of said predetermined bit of said substitutive address;

an address selector for receiving determination results of said address comparator, outputting as a value of said predetermined bit of a new instruction address, the value held in said substitutive address storage unit when the received results indicate that these values match with each other, and otherwise, the value of said predetermined bit of the instruction address; and

a translation range setting means capable of setting whether or not said predetermined bit is designated as a translation target bit, said translation range setting means making said address selector output the value of said predetermined bit of the instruction address, regardless of the determination results of said address comparator when said predetermined bit is not designated as the translation target bit.

5. The microprocessor of claim 1, wherein said address translation unit is composed of a memory which outputs translated addresses in accordance with received instruction addresses.

6. The microprocessor of claim 1, wherein said address translation unit is composed of a field programmable logic which outputs translated addresses in accordance with received instruction addresses.

7. The microprocessor of claim 1, wherein said modified instruction storage unit stores an additional instruction for program modification and further stores a branch instruction at the substitutive address, the branch instruction having as a branch target an address of the additional instruction.

8. A method for program modification in a microprocessor provided with an instruction storage unit including a ROM for storing instructions composing a program to be processed and a modified instruction storage unit for storing a modified instruction for program modification, comprising the steps of:

comparing an instruction address of an instruction stored in said ROM with a modifying address which is an address of an instruction to be modified;

translating the instruction address into a substitutive address at which the modified instruction is stored in said modified instruction storage unit when the instruction address and the modifying address match with each other; and

providing said instruction storage unit with the substitutive address instead of the instruction address.

9. The method of claim 8 further comprising the steps of, before said address comparison,

storing an additional instruction for program modification to said modified instruction storage unit; and

storing a branch instruction at the substitutive address, the branch instruction having as a branch target an address of the additional instruction.